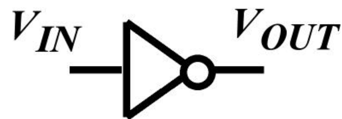
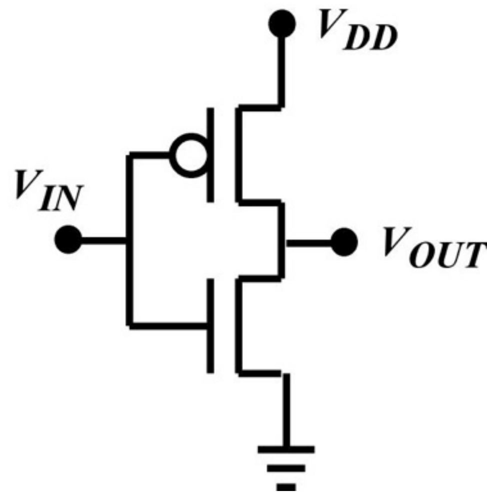
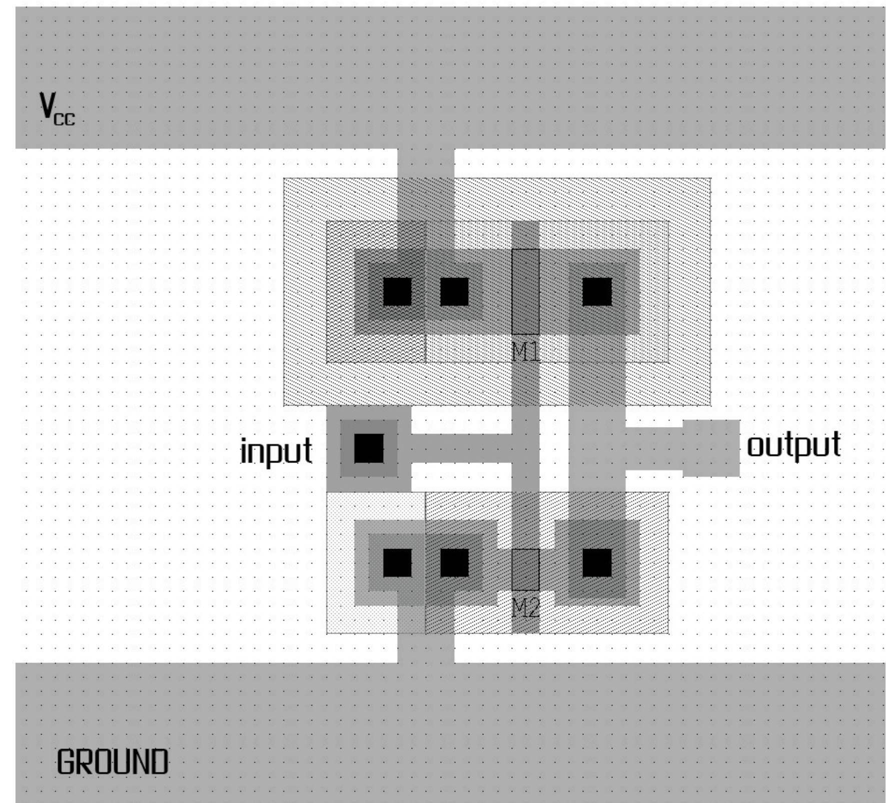
6.4, 6.5 – Real MOSFET, Inverters, Capacitance

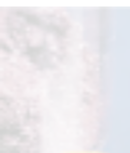
14 pin 'Hex' inverter:
6 inverters I/O pins (12)
1 V_{DD} , 1 GND (2)

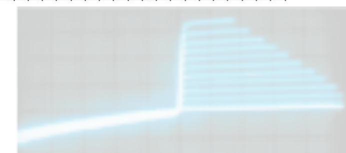


V_{IN}	V_{OUT}
0V	5V
5V	0V

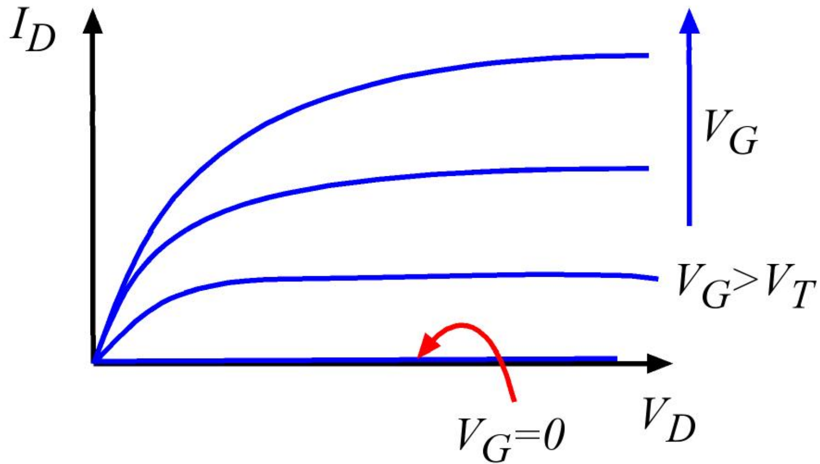


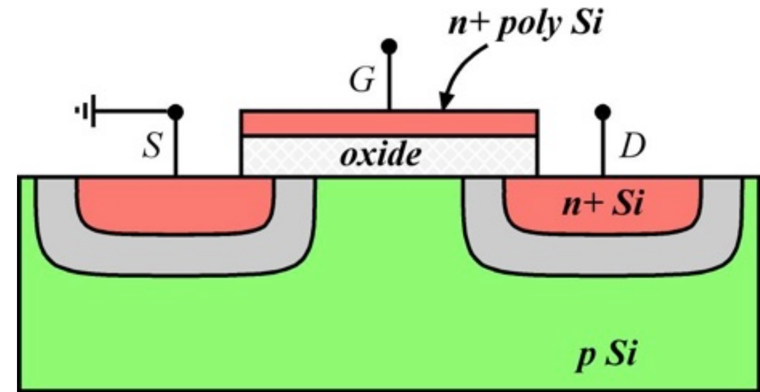






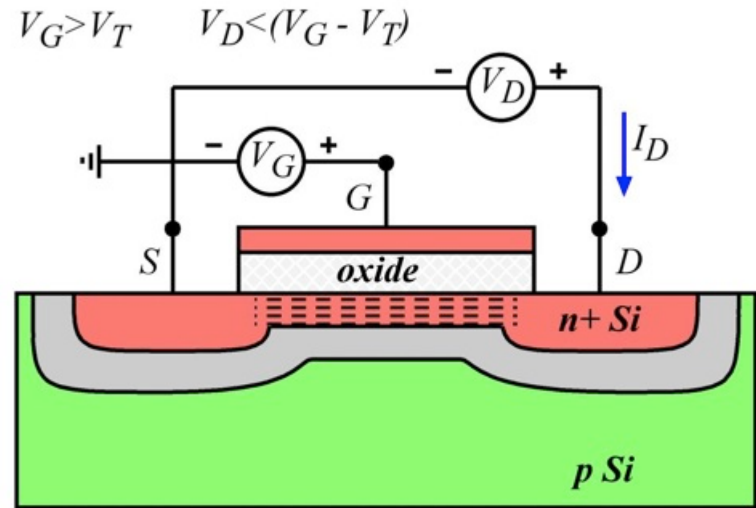
- Bringing it all together (review)



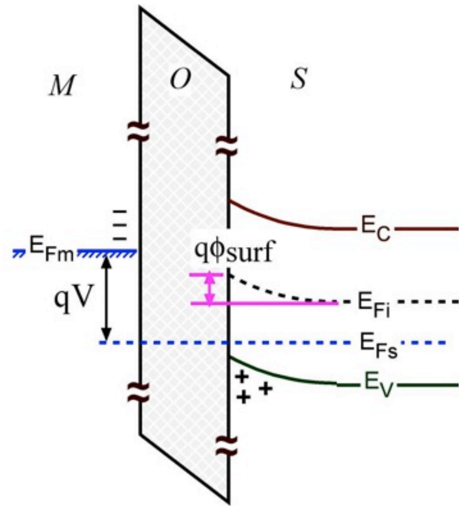


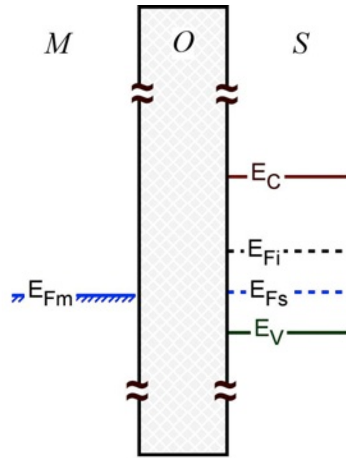
- The depletion I can create under the gate oxide maximizes, why?

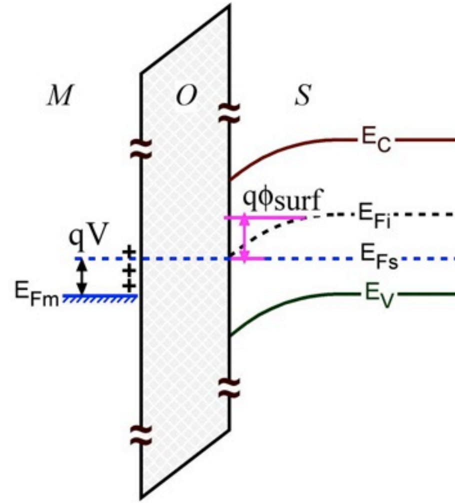
- Once above threshold voltage, at what mathematical rate are carriers created in the channel?

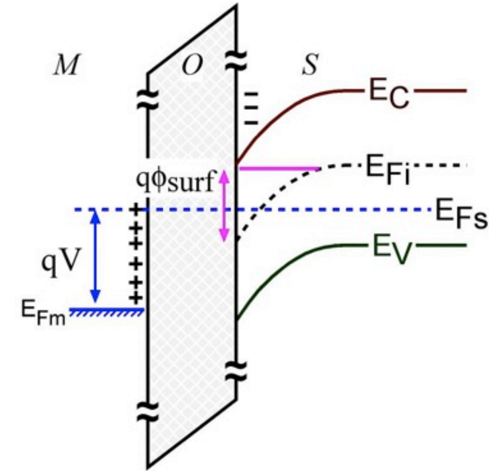


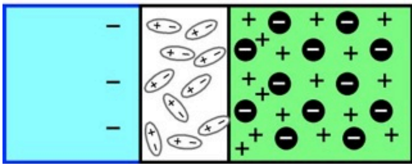
- Accumulation
- Flat Band
- Depletion & Weak Inversion
- Inversion

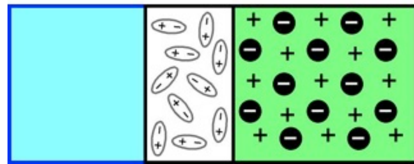


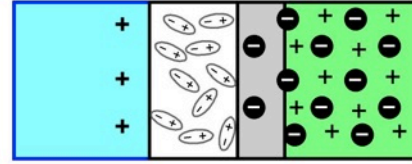




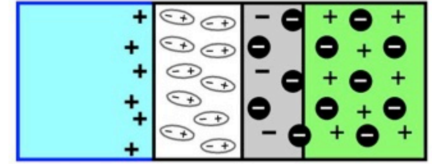


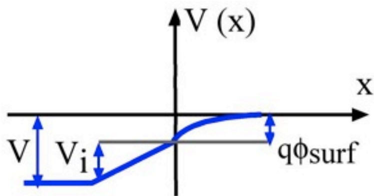


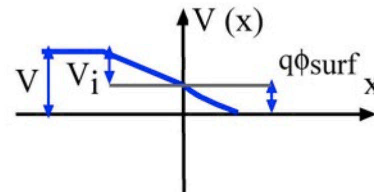


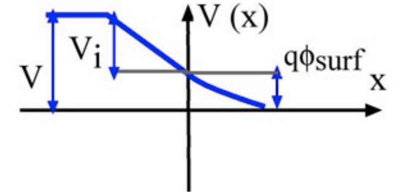


charge, but no channel!





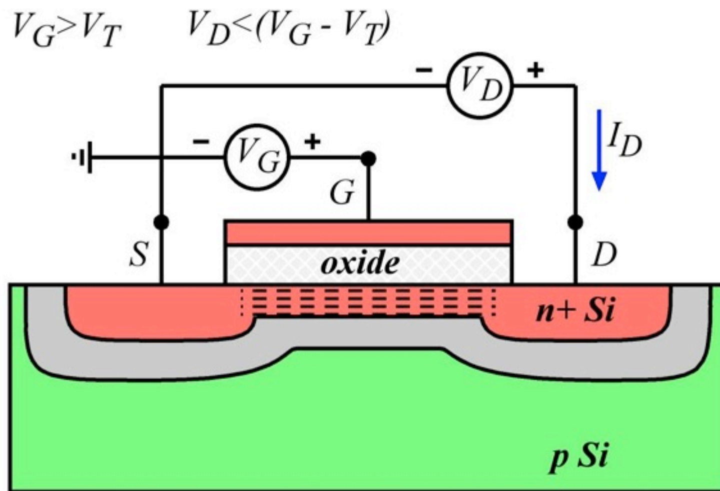


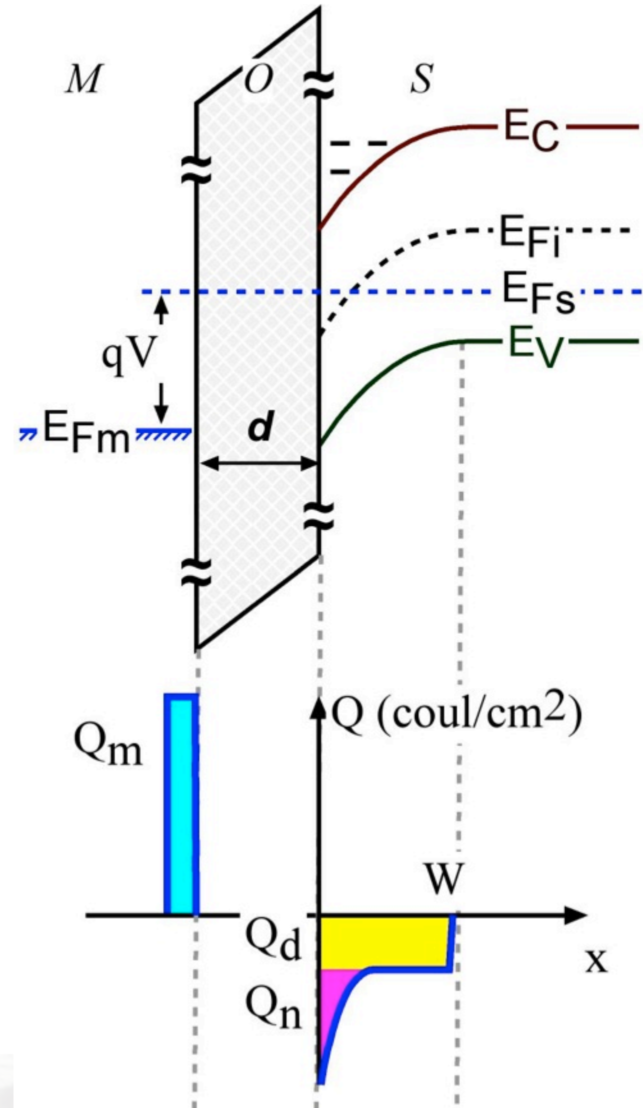


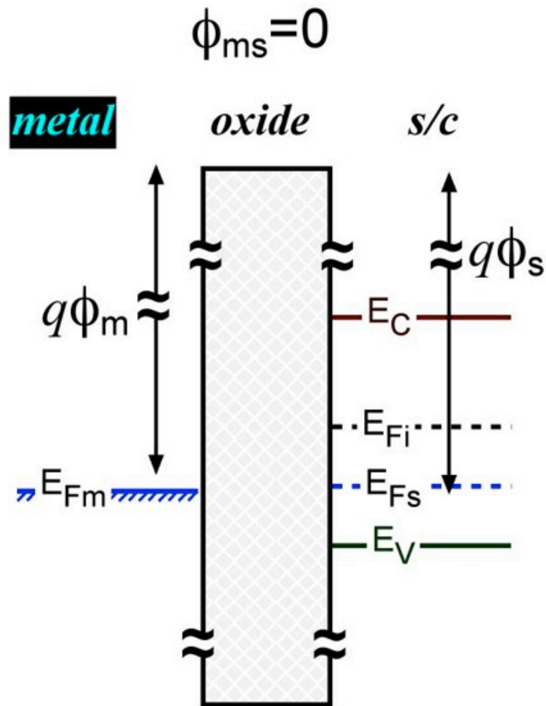
IDEAL CASE: $V_T = -\frac{Q_{d,\max}}{C_i} + 2\phi_f$

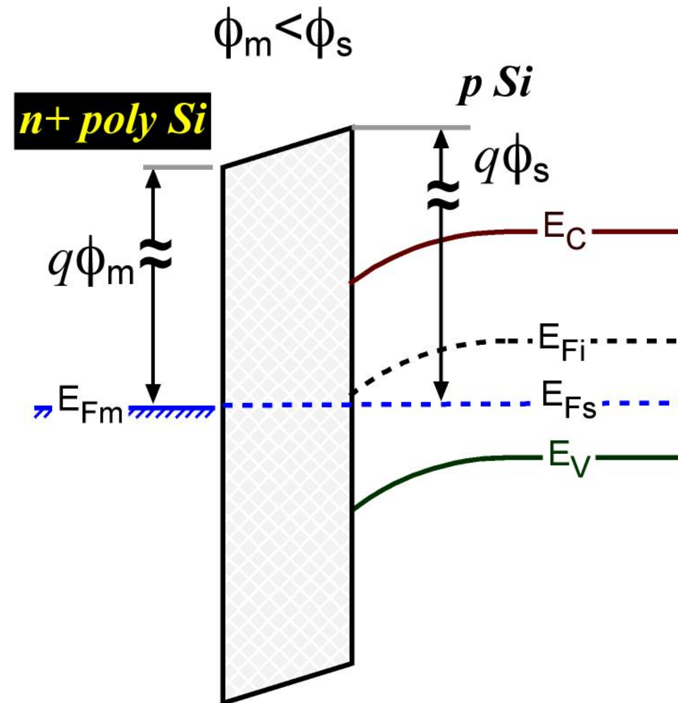
1) deplete holes $Q_{d,\max} = -2\sqrt{\varepsilon_s q N_a \phi_F}$

2) get inversion (electrons and n-channel) $\phi_F = \frac{kT}{q} \ln \frac{N_a}{n_i}$







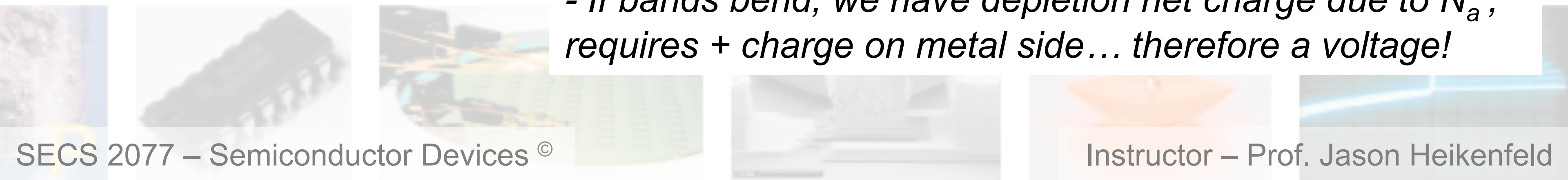


- This is for V=0 (thermal equilibrium!, look at the Fermi levels…)

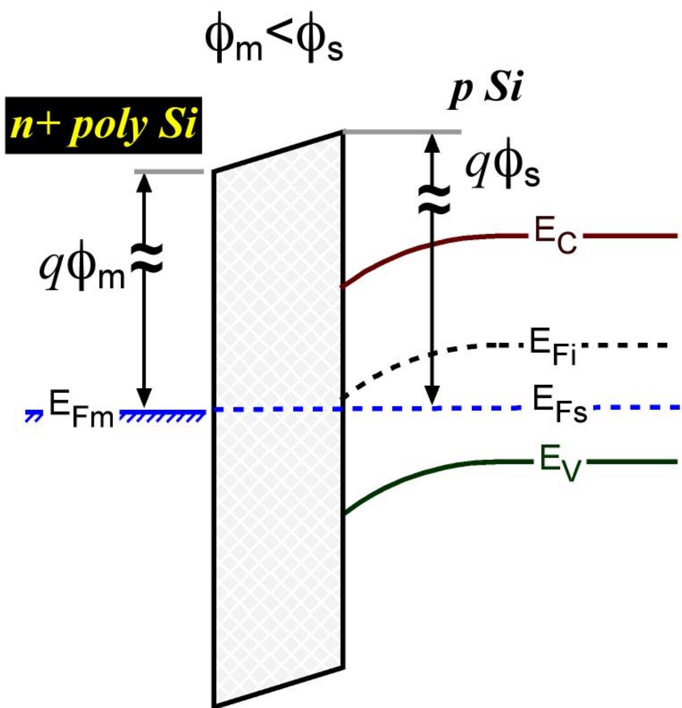
- Why do the bands and oxide bend?

- Fermi levels line up, metal like n++ so all bend on Si side

- If bands bend, we have depletion net charge due to N_a^-, requires + charge on metal side… therefore a voltage!



- Let start to develop the REAL threshold voltage for n-hannel MOSFETs



IDEAL CASE: $V_T = -\frac{Q_{d,\max}}{C_i} + 2\phi_f$

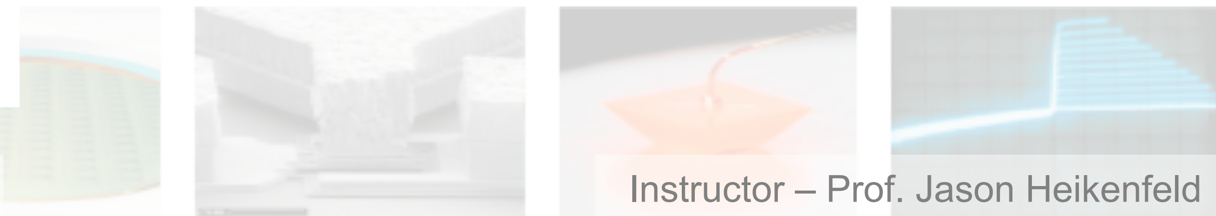
1) deplete holes $Q_{d,\max} = -2\sqrt{\varepsilon_s q N_a \phi_F}$

2) get inversion (electrons and n-channel) $\phi_F = \frac{kT}{q}\ln\frac{N_a}{n_i}$

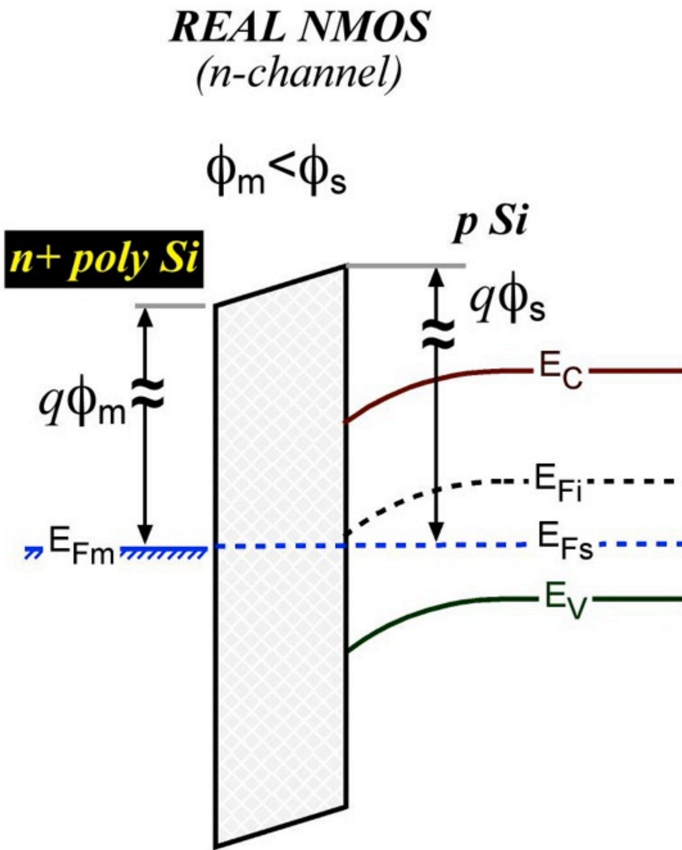
REAL CASE: $V_T = \phi_{ms} - \frac{Q_{d,\max}}{C_i} + 2\phi_f$

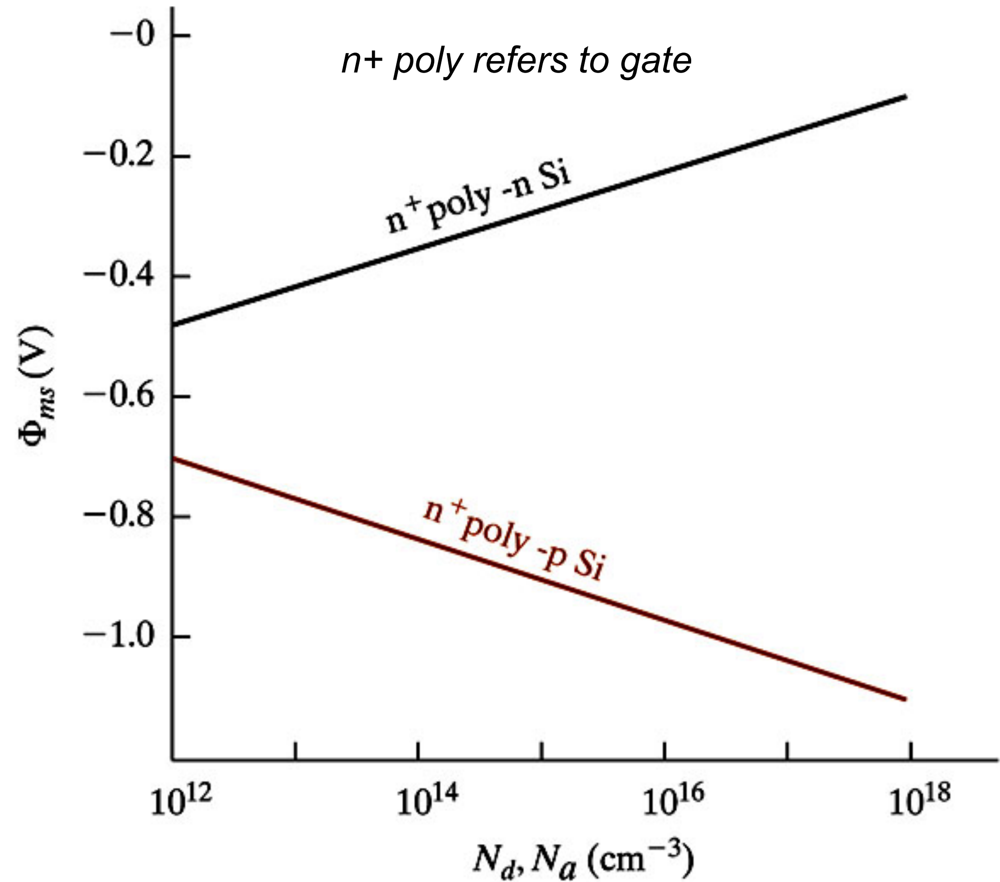
3) Built in potential $\phi_{ms} = \phi_m - \phi_s$

For this example does this lower or raise our V_T? Can do this by looking at the equation or the bands…



- Look at $\phi_{ms} = \phi_m - \phi_s$ in more detail...



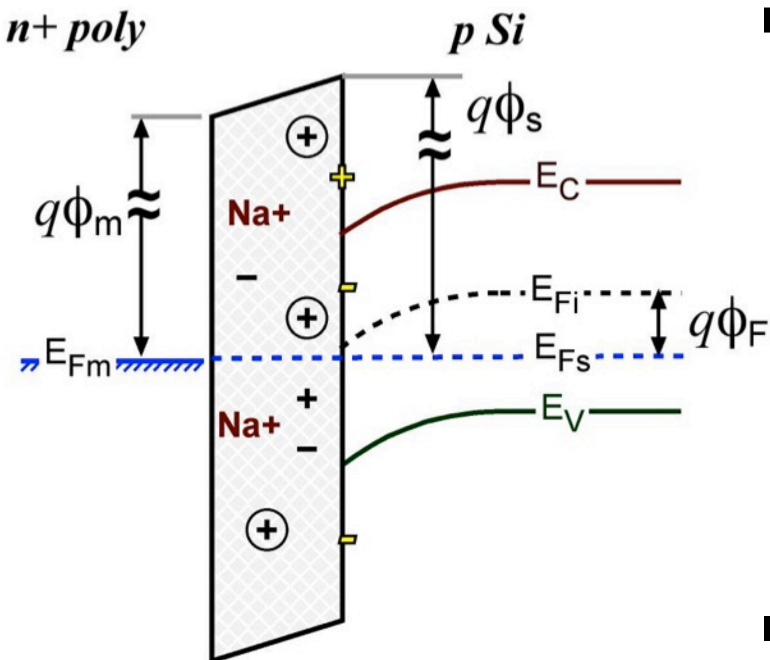


We can't change ϕ_m but we can change ϕ_s

- more p-type, Ef ↓ , $|\phi_{ms}|$ ↑
- more n-type, Ef ↑ , $|\phi_{ms}|$ ↓

$$V_T = \phi_{ms} - \frac{Q_{d,\max}}{C_i} + 2\phi_f$$

- We are not done yet! There are more non-ideal effects…



1) deplete holes $Q_{d,\max} = -2\sqrt{\varepsilon_s q N_a \phi_F}$

2) get inversion (electrons and n-channel) $\phi_F = \frac{kT}{q} \ln \frac{N_a}{n_i}$

3) Built in potential $\phi_{ms} = \phi_m - \phi_s$

REAL CASE: $V_T = \phi_{ms} - \frac{Q_{d,\max}}{C_i} + 2\phi_f$

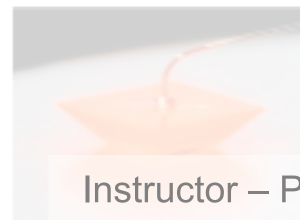
Couple types of charge: ionic, oxide, oxide/Si interface.

Oxide/Si interface charge often dominates and is often + (which attracts e-, means bands must bend down).

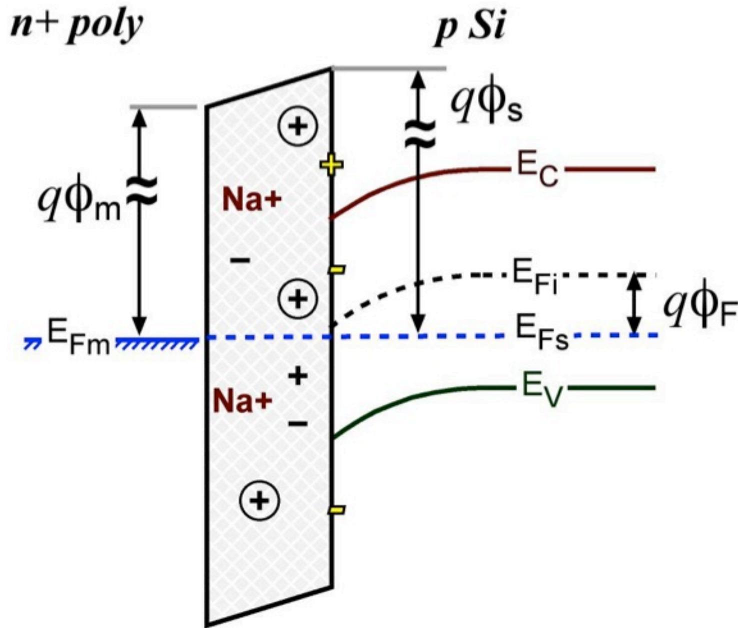
How will we add it to our V_T equation?

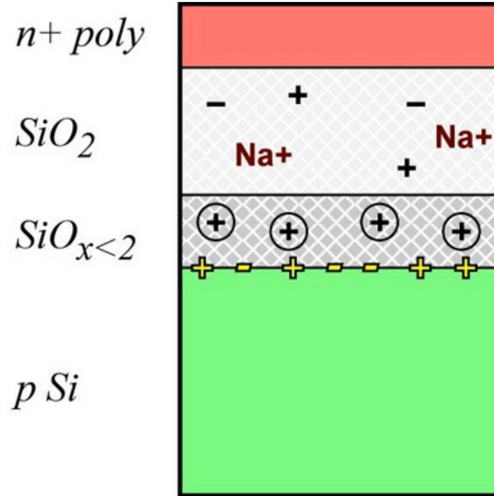
4) Interface Charge Q_i

REAL CASE: $V_T = \phi_{ms} - \frac{Q_i}{C_i} - \frac{Q_{d,\max}}{C_i} + 2\phi_f$



- Look at *Qi in more detail*

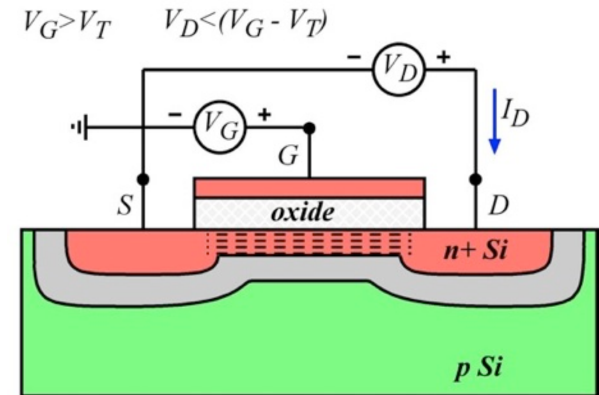




Q_i is made of all these…

- Q_{ot}=oxide trapped charge
- Na+ Q_m=mobile ionic charge
- Q_f=oxide fixed charge
- Q_{it}=interface trap charge

Q_f dominates!



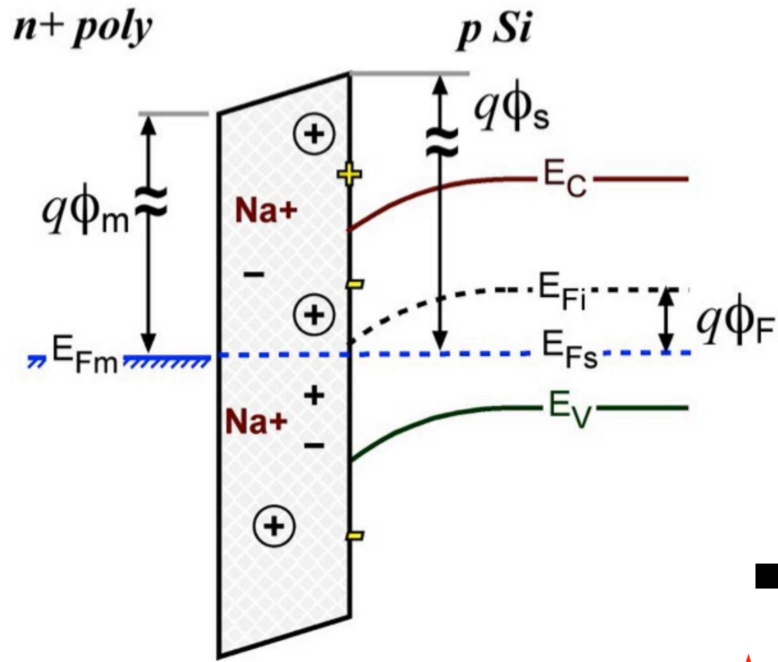
Due to Q_f, the net Q_i is positive charge, pulls band down (lower V_T).

Don't get confused, Q_d increases V_T since it is a negative charge!

$$V_T = \phi_{ms} - \frac{Q_i}{C_i} - \frac{Q_{d,\max}}{C_i} + 2\phi_f$$

- Now we have the full story! Lets review…

IDEAL CASE: $V_T = -\frac{Q_{d,max}}{C_i} + 2\phi_f$



1) deplete holes $Q_{d,max} = -2\sqrt{\varepsilon_s q N_a \phi_F}$

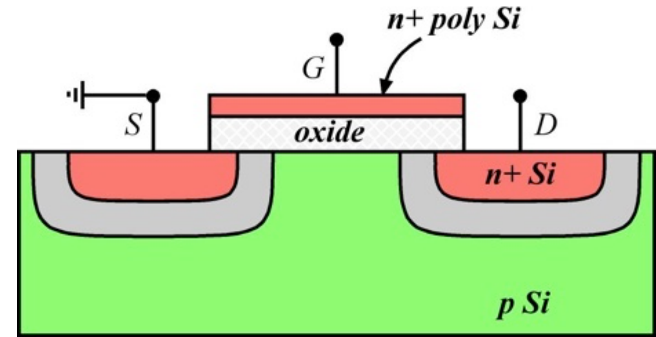
2) get strong inversion (electrons and n-channel) $\phi_F = \frac{kT}{q}\ln\frac{N_a}{n_i}$

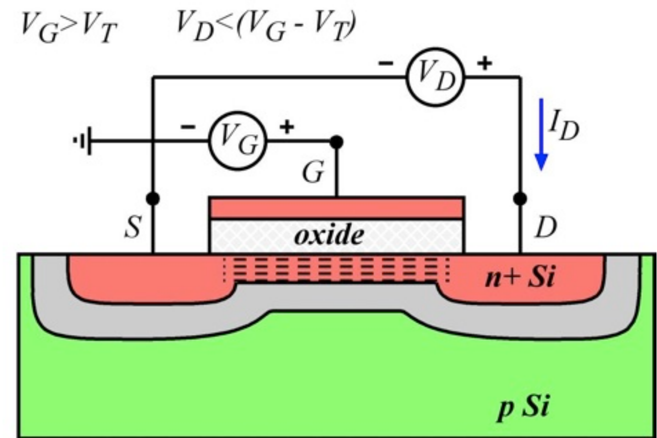
3) workfunctions $\phi_{ms} = \phi_m - \phi_s$

4) interface charge Q_i

REAL CASE: $V_T = \phi_{ms} - \frac{Q_i}{C_i} - \frac{Q_{d,max}}{C_i} + 2\phi_f$

- What factors are needed for the ideal V_T and do they increase or decrease V_T?
- What factors are needed for the real V_T and do they increase or decrease V_T?
- What factors for the real V_T will change with doping level in the p Si substrate? *Hint, there are 3 of them…*
- Φ_{ms} , for a n+ polycrystaline Si gate and a n+ substrate underneath the gate it should be approximately what? *This should be easy!*



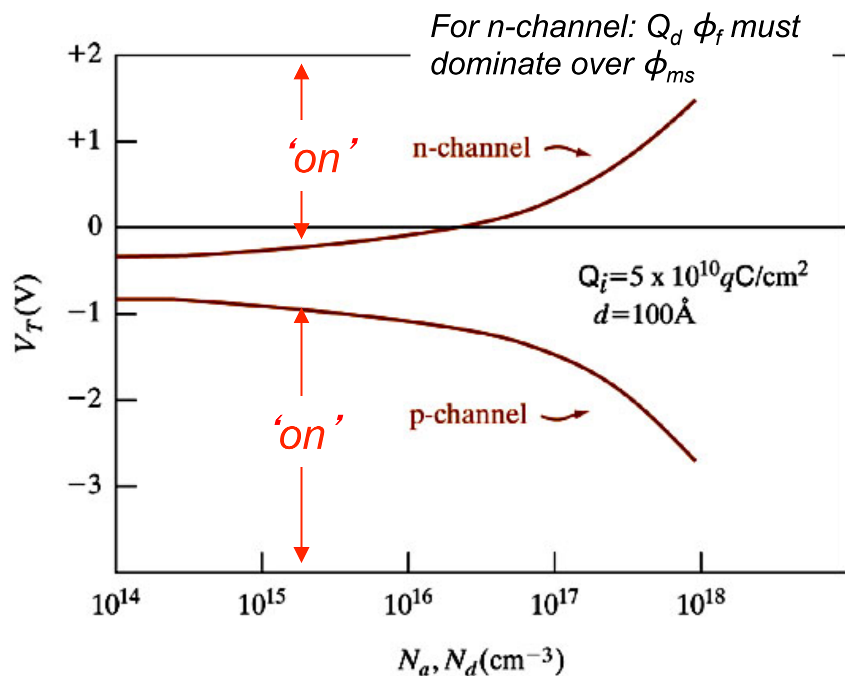


$$V_T = \phi_{ms} - \frac{Q_i}{C_i} - \frac{Q_{d,\max}}{C_i} + 2\phi_f$$

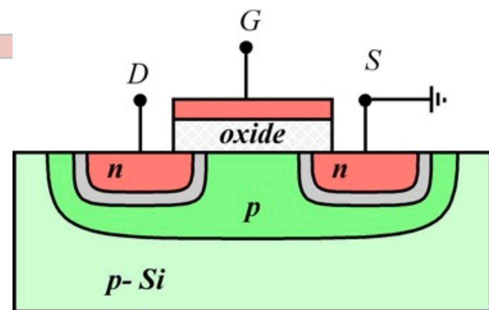
$$g_m(sat.) = \frac{\partial I_D(sat.)}{\partial V_G}$$

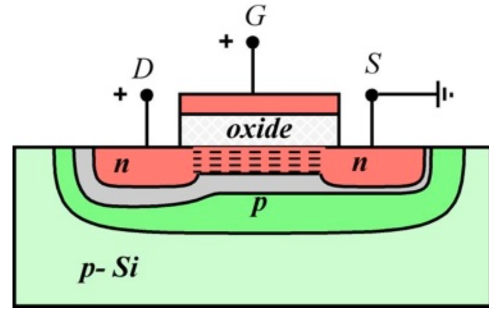
$$V_T = \phi_{ms} - \frac{Q_i}{C_i} - \frac{Q_{d,max}}{C_i} + 2\phi_f$$

shifts — flip +/- for PMOS



- NMOS
  - -n-channel
  - -*enhancement*

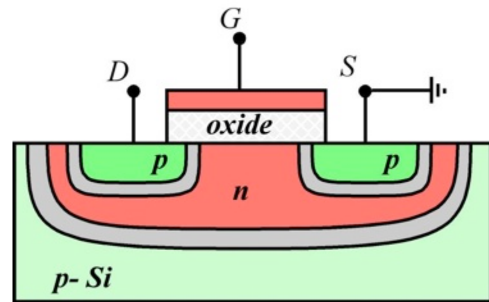


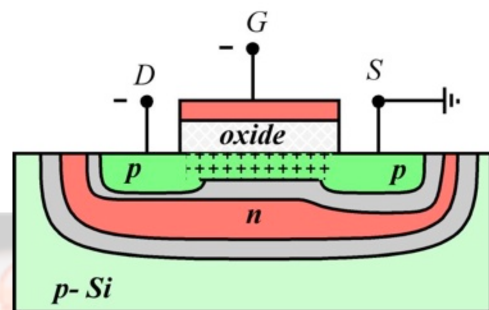


- PMOS
  - -p-channel
  - -*enhancement*

Why p-Si substrate?

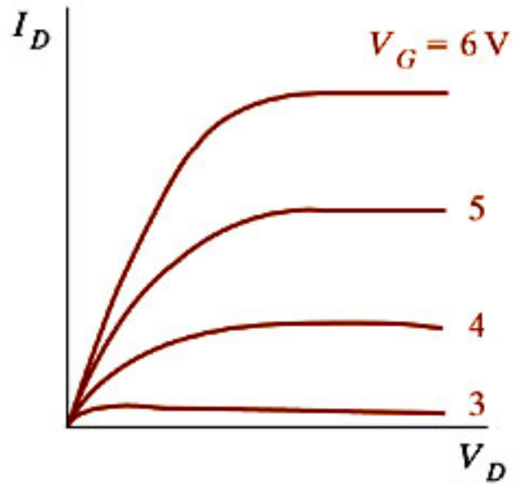
In V_T equation at above left, shifts or flips V? ☆



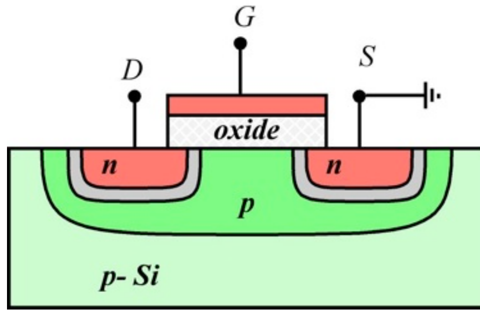


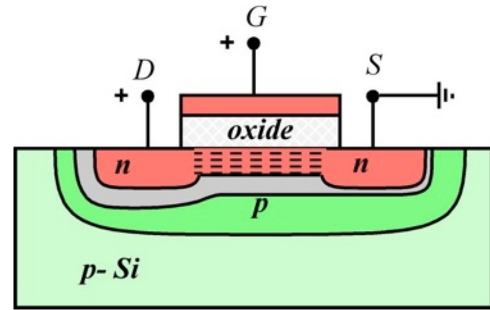
Note Φ_{ms} and Q_i cause N-MOS to be 'on' at 0V…

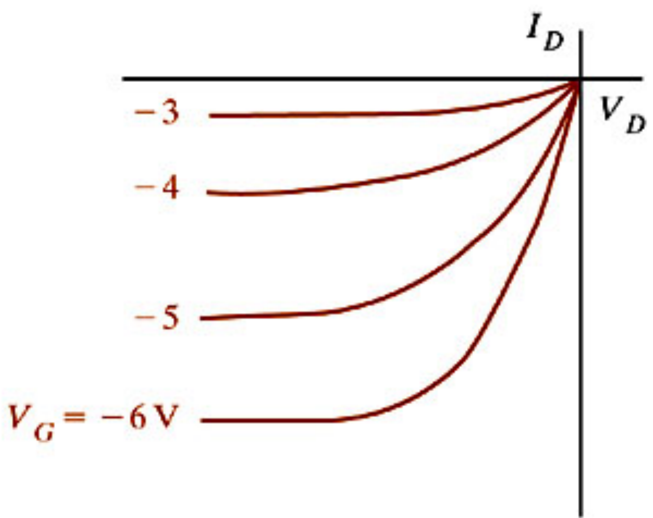
… *therefore in real MOS they must make some materials/device modifications or DC offsets. Otherwise it would be 'depletion mode'.*



- NMOS
-n-channel
-enhancement

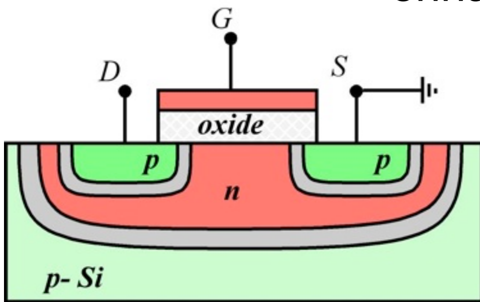


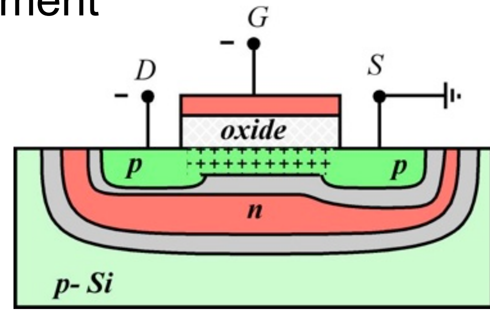




- PMOS
-p-channel
-enhancement

OOPS – Depletion drawn incorrect!

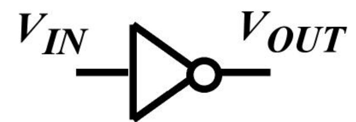




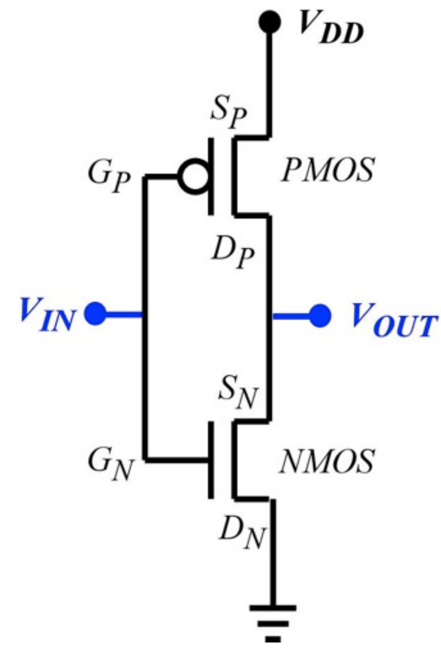
Note, they made V_D negative (you will see in two slides why they do this for an inverter…)

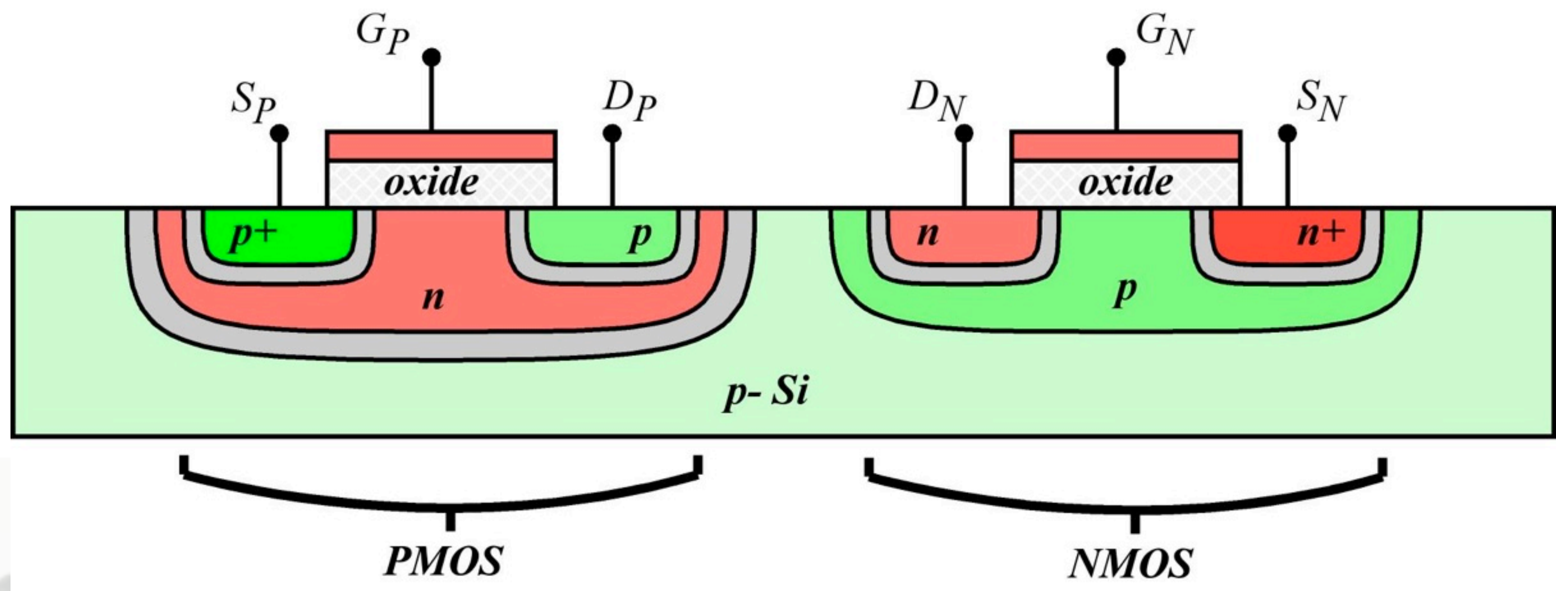
- Recall from earlier coursework

INVERTERS, BUFFERS (repeater), AND, OR, NAND (inverted AND), NOR (inverted OR), XOR (one or the other, only), etc.. *that these devices all use complementary MOS (CMOS)!*



V_{IN}	V_{OUT}
0V	5V
5V	0V





CMOS (Complementary MOS)

V_{DD} S D $I_{DP} = I_{DN}$ V_{in} V_{out} D C S

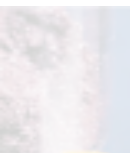
(a)

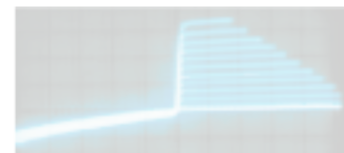
I_D NMOS $V_{in} = V_{DD}$ PMOS $V_{in} = 0$ NMOS, $V_{in} = 0$ PMOS $V_{in} = V_{DD}$ 0 V_{DD} $V_D\,(V_{out})$

(b)

- This is a plot of the total current at Id for the PMOS (blue dotted line) and the NMOS (black line) vs. Vd….

It basically shows you that you want to lock Vd into a 0 or a 1, not in between, because then current flows through both transistors!



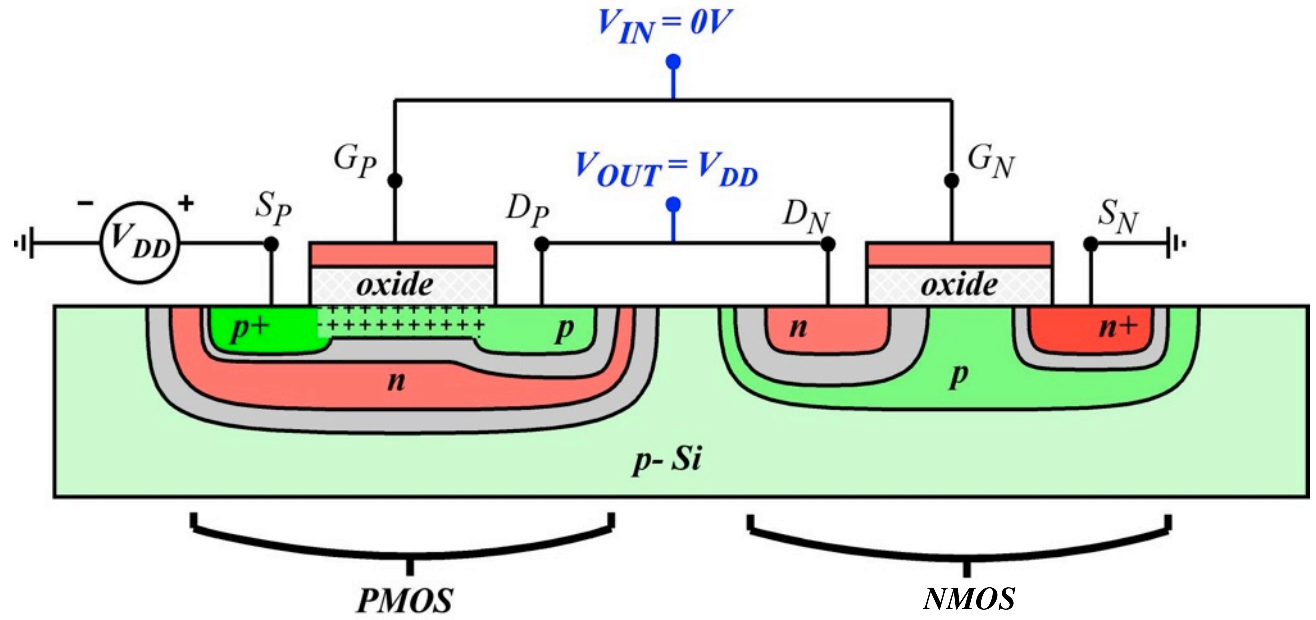


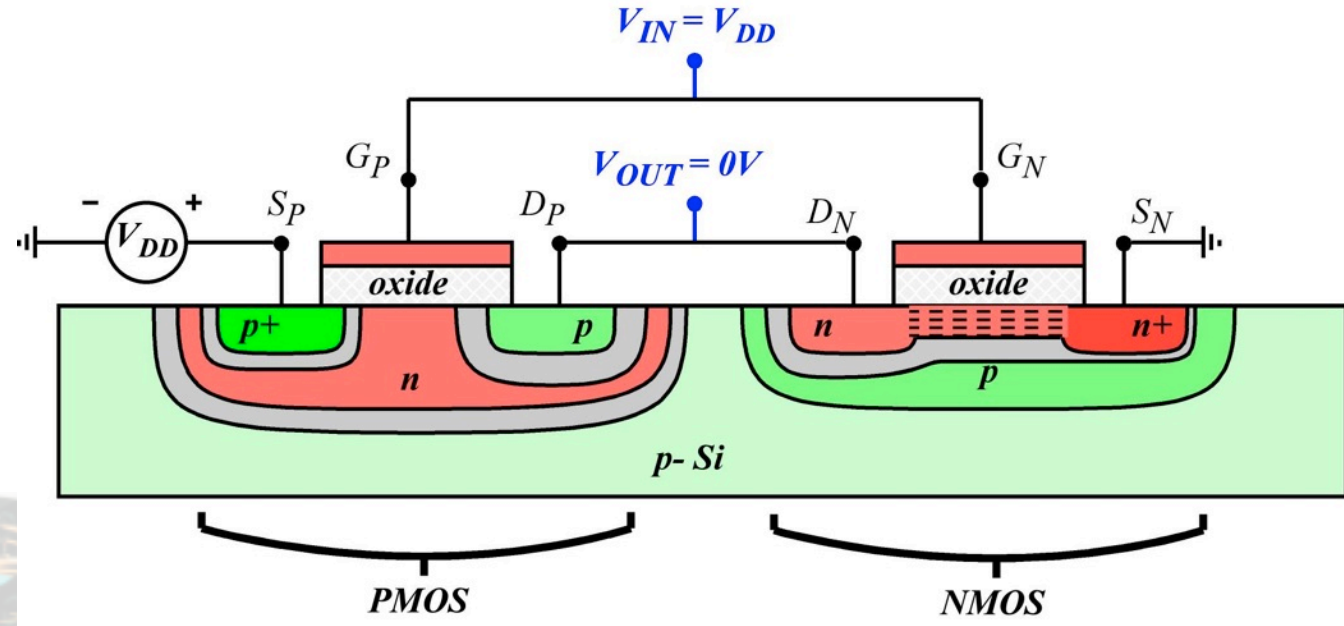
1) assume ideal case

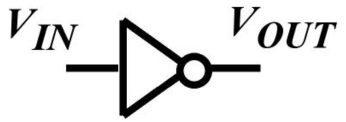
2) Note how the source biases the semiconductor beyond the source but does not effect the adjacent FET

- *Can you label the voltages at all locations?* ☆

3) note the depletion region widths…



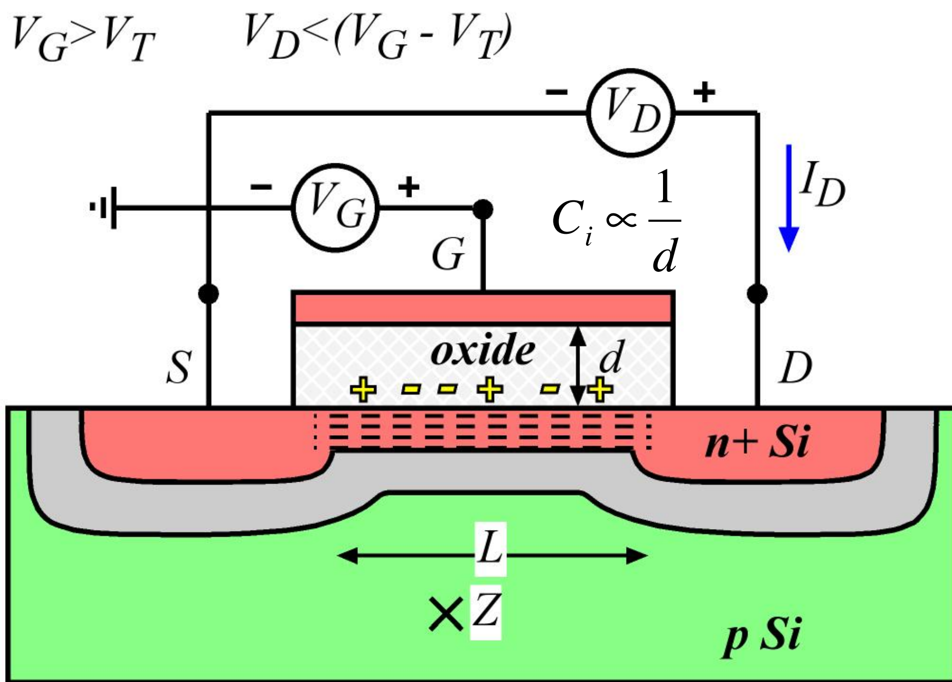




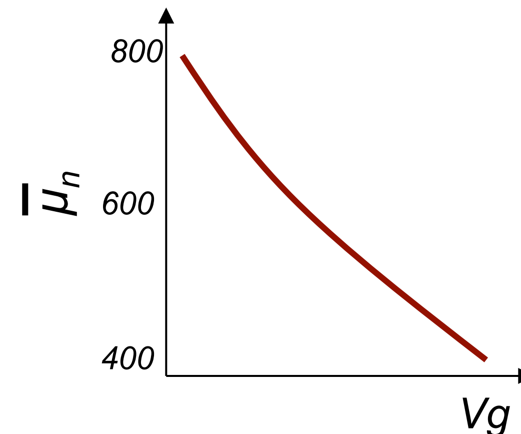
V_{IN}	V_{OUT}
0V	5V
5V	0V

- It can be shown (6.5.1) that the NMOS drain current at <u>low</u> V_D (not satur.) is:

$$I_d = \frac{\bar{\mu}_n Z C_i}{L}\left[(V_G - V_T)V_D - \frac{1}{2}V_D^2\right]$$



- Larger current is often good for fast switching (RC)… look at equation at left and examine these factors:
  - *- shorter channel length (L)*
  - *- larger channel width (Z)*
  - *- thinner oxide layer (C_i)*
  - *- lower threshold voltage (V_T)*
  - *,and…*
  - *- higher <u>surface</u> e mobility ($\bar{\mu}_n$)*

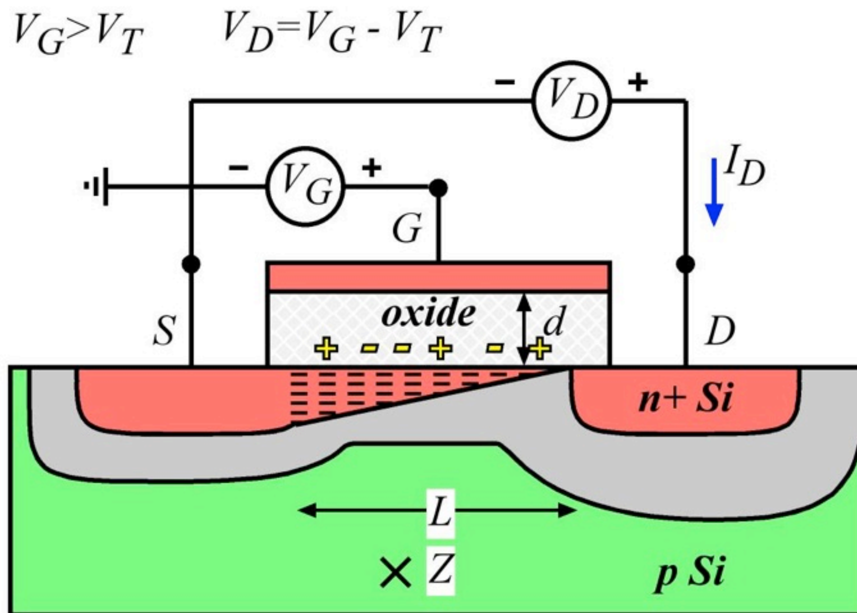


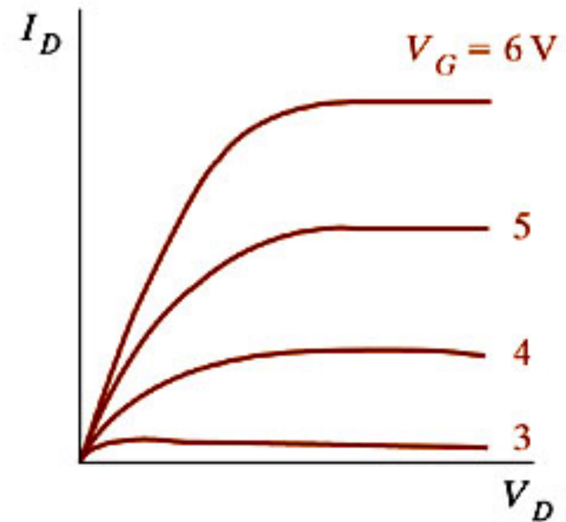
μ_n is ~1300 for Si…
and $\bar{\mu}_n$ lower due to roughness and fixed charge at oxide/Si interface… *but why decrease with increasing Vg?* ☆

- It can be shown (6.5.1) that NMOS drain current for all V_D values including pinch-off (saturation) is given by:

$$I_d = k_N\left\{\left(V_G - V_{FB} - 2\phi_F - \frac{1}{2}V_D\right)V_D - \frac{2}{3}\frac{\sqrt{2\varepsilon_s q N_a}}{C_i}\left[(V_D + 2\phi_F)^{3/2} - (2\phi_F)^{3/2}\right]\right\}$$

$$k_n = \frac{\overline{\mu}_n Z C_i}{L}$$ (transconductance parameter)





- For NMOS in linear region where $V_D << (V_G-V_T)$

$$I_d = \frac{\bar{\mu}_n Z C_i}{L}\left[(V_G - V_T)V_D - \frac{1}{2}V_D^2\right]$$

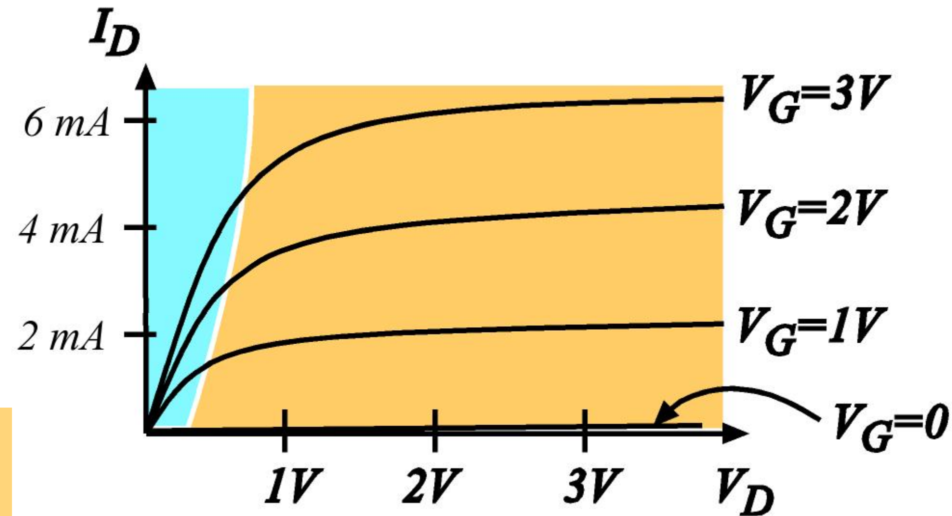
- At saturation, no point in having effect of V_D in equation, so new term $V_{D,Sat.} \approx (V_G-V_T)$

$$I_d(\text{sat.}) \approx \frac{1}{2}\frac{\bar{\mu}_n Z C_i}{L}V_{D,Sat.}^2$$

- An important parameter for MOSFETs is their transconductance: g_m(sat.)

$$g_m(sat.) = \frac{\partial I_D(sat.)}{\partial V_G}$$

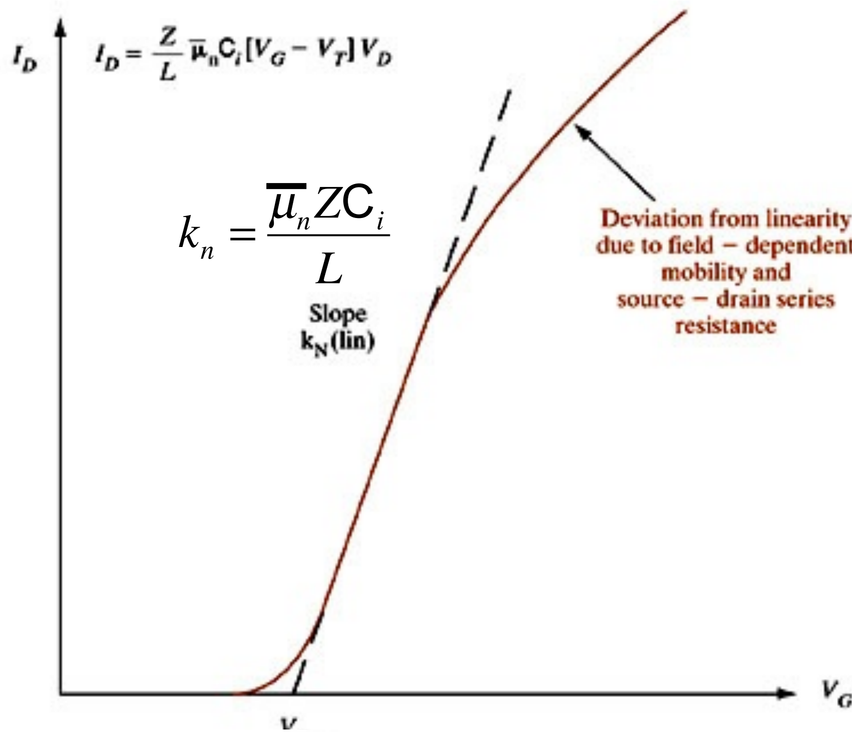
$$g_m(sat.) \approx \frac{\bar{\mu}_n Z C_i}{L}(V_G - V_T)$$

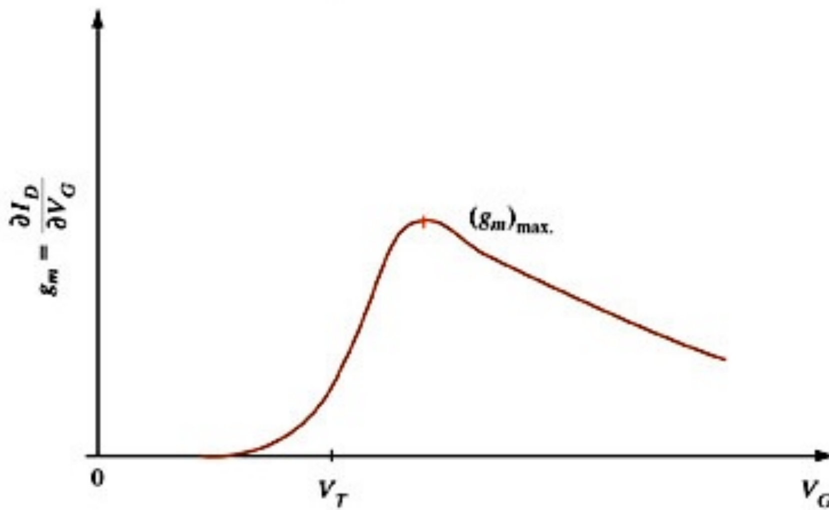


- *What is g_m for the curves above?*

g_m = (4-2 mA)/(2-1)V

$g_m = 2x10^{-3}$ mhos





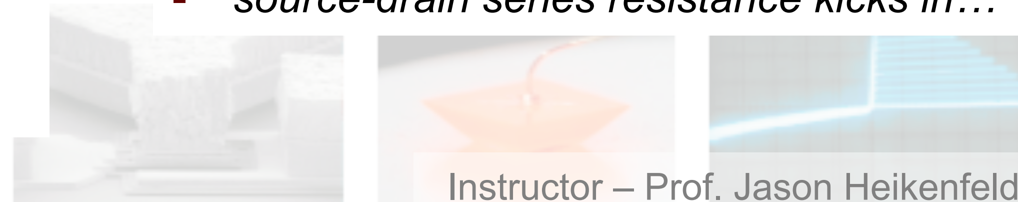
$$I_d = \frac{\bar{\mu}_n Z C_i}{L}\left[(V_G - V_T)V_D - \frac{1}{2}V_D^2\right]$$

We showed previously that inversion Q increases exponentially with surface potential (ϕ_s). However, that does not represent *externally* applied voltage (V_G), where inversion Q (and conduction) will be linear due to Q=CV_G… ☆

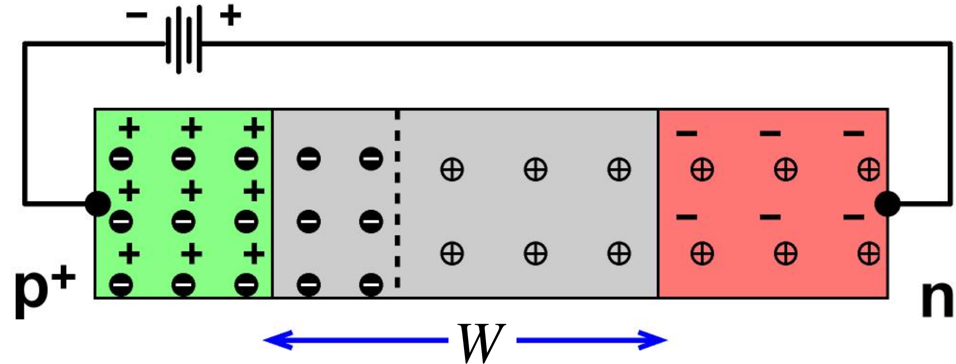
$$g_m(sat.) = \frac{\partial I_D(sat.)}{\partial V_G} \cong \frac{\bar{\mu}_n Z C_i}{L}(V_G - V_T)$$

Lets look at g_m vs. Vg in saturation…

- First g_m increases as you create the channel
- Then g_m then fades as
  - *surface mobility decreases with increased Vg*
  - *source-drain series resistance kicks in…*

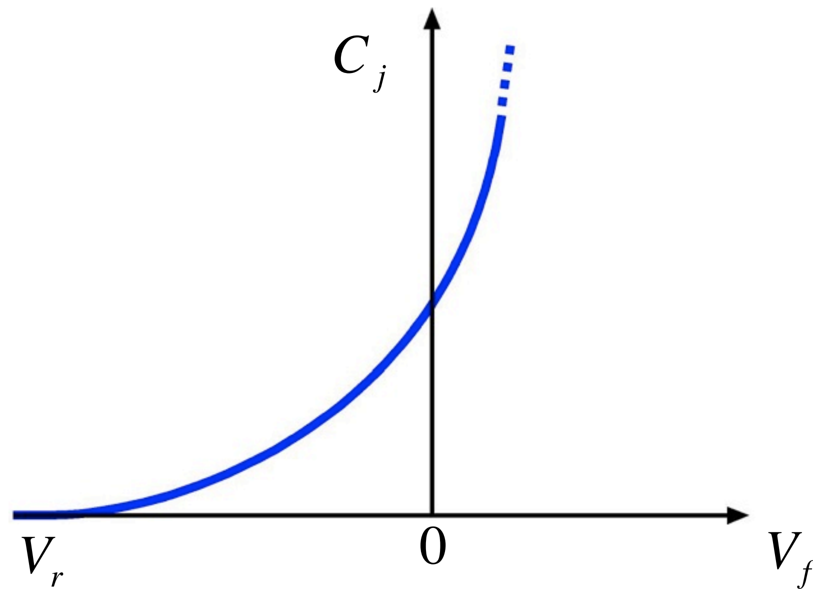


- Lets look at MOSFET Capacitance… (last topic)

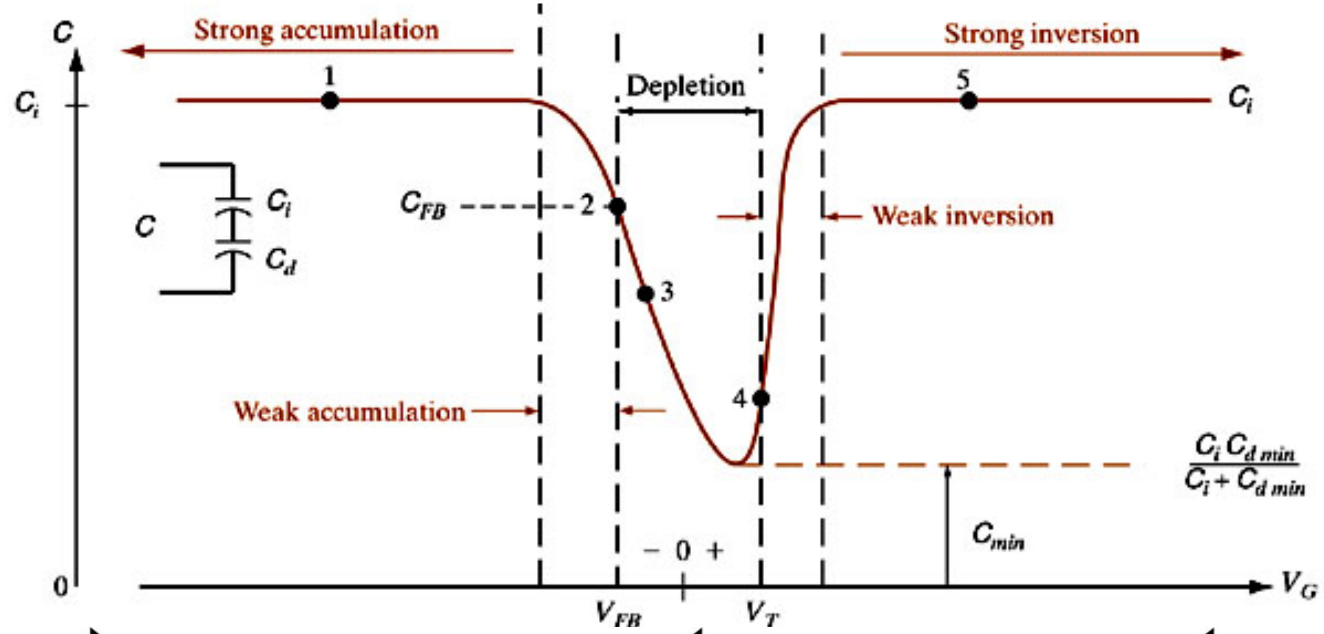


- Recall that for a PN junction capacitance decreases with reverse bias voltage… (why?).

$$C_j = \frac{\varepsilon A}{W} = \frac{\varepsilon_0 \varepsilon_{Si} A}{W}$$



- We should then expect a similar effect for the MOS capacitor, however… we also have to deal with accumulation and inversion!



M O S
E_{Fm} E_C E_{Fi} E_{Fs} E_V

M O S
E_{Fm} E_C E_{Fi} E_{Fs} E_V

M O S
E_{Fm} E_C E_{Fi} E_{Fs} E_V

Strong accumulation
Strong inversion
Depletion
Weak inversion
Weak accumulation
C, C_i, C_{FB}, C_d, C_{min}, V_{FB}, V_T, V_G
1 2 3 4 5
$- \; 0 \; +$

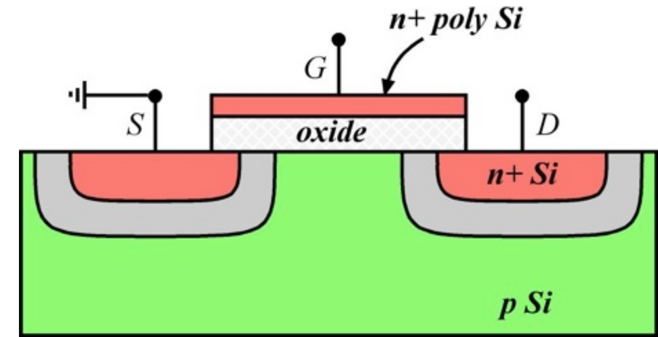
$$\frac{C_i C_d}{C_i + C_d}$$

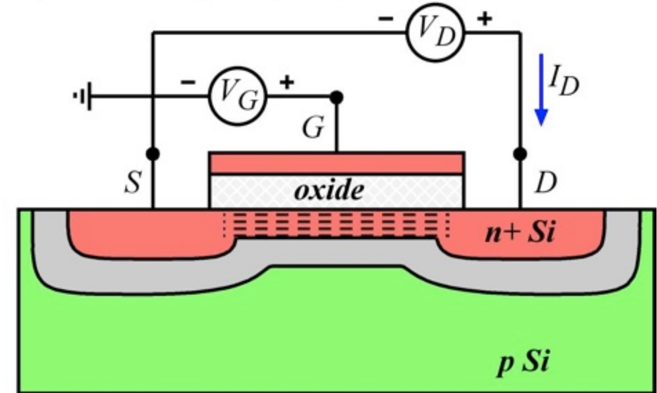
C_d non-existent, like a metal/insulator/metal (MIM) capacitor

depletion causes C_d to appear and become low in capacitance

C_d is max, but inversion charge at the oxide surface makes this look like a MIM capacitor again, note that this is for ***LOW FREQ*** *(we won't go into the details)*

- What terms for V_T invert in sign for PMOS? (devices at right are NMOS)
- What terms for V_T shift for PMOS?
- Roughly, what is the voltage in the p Si substrate for the device with voltage sources on it?
- How will the MOSFET capacitance change with V_G? *There are three factors/regions of capacitance…*
- Is drain current vs. gate voltage (called transfer characteristic) linear or exponential, and what fundamental 3-variable equation determines why?

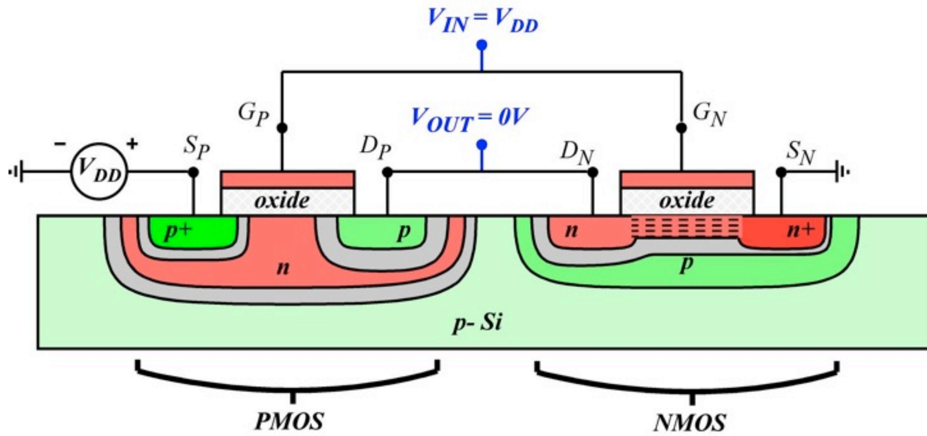


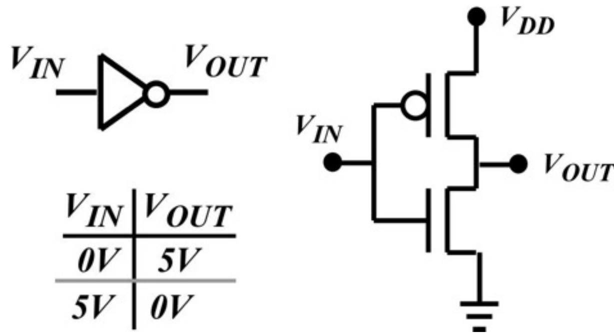


$$V_T = \phi_{ms} - \frac{Q_i}{C_i} - \frac{Q_{d,\max}}{C_i} + 2\phi_f$$

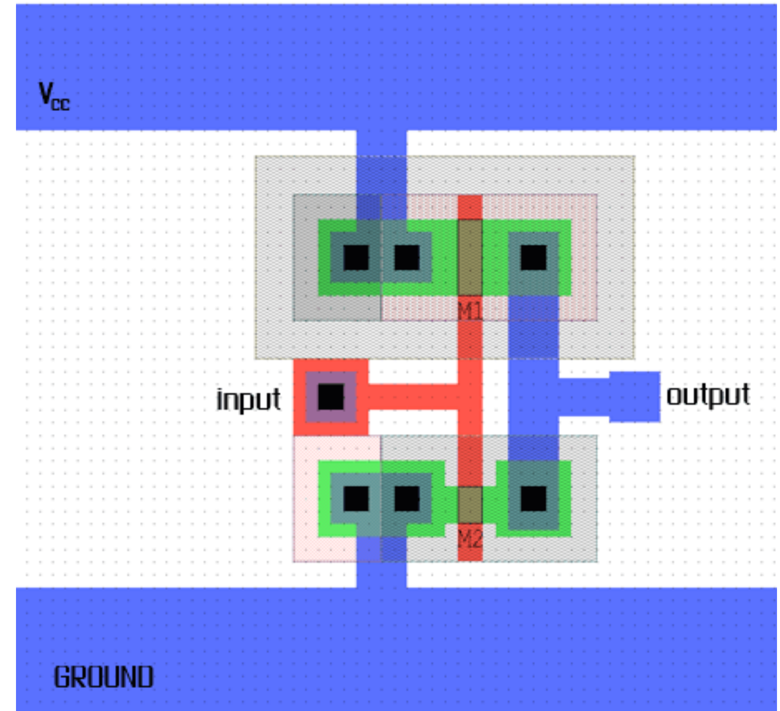
$$g_m(sat.) = \frac{\partial I_D(sat.)}{\partial V_G}$$

- This is an inverter…. will tell you next time what the layers are :)





V_{IN}	V_{OUT}
0V	5V
5V	0V



www.sccs.swarthmore.edu/users/06/adem/engin/e77vlsi/lab3/

Funny, I randomly picked my colors for materials when starting this course and they seem to match up!